AMENDMENTS TO THE SPECIFICATION

Please amend the specification at page 12, line 1 to line 7 to read as follows:

~~Figure 2A~~ Section A of Figure 2 illustrates a sensor package wherein two horizontal, 1-dimensional, sensor circuit components are mounted separately in space on the PCB, with only one of the two sensor circuit components serving as a support for the vertical sensor circuit component 103. ~~Figure 2B~~ Section B of Figure 2 illustrates a sensor package wherein the two horizontal, 1-dimensional, sensor circuit components 204 are in contact, conductively or non-conductively attached, with both serving as a support for the vertical sensor circuit component 103.

Please amend the specification at page 14, line 20 to page 15, line 1 to read as follows:

Such exemplary electrical connections are represented by wire bonds or TAB bonds 105 between the horizontal sensor circuit component 102, 204 and the PCB 101 in section A of Figure 3 ~~Figure 3 (A)~~, solder joints 105 between the vertical sensor circuit component 103 and the PCB 101 in sections A and C of Figure 3 ~~Figure 3 (A) and (C)~~, and stud bumps encased in conductive epoxy 105 between the vertical sensor circuit component 103 and the PCB 101 in section B of Figure 3 ~~Figure 3 (B)~~.

Please amend the specification at page 16, line 22 to page 17, line 1 to read as follows:

Similarly, for embodiments such as that illustrated in section B of Figure 2 ~~Figure 2(B)~~, any of the sensor components 103, 204 can be in direct electrical communication with any other sensor component to which it is abutted.

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Please amend the specification at page 18, line 5 to line 13 to read as follows:

Similarly, a sensor component fixture 107 can be utilized with embodiments such as that illustrated in section B of Figure 2 ~~Figure 2(B)~~, wherein all sensor components 103, 204 are in direct electrical or non-electrical communication. As with Figures 4 and 5, the methods of forming electrical interconnections 105 outlined above are preferably utilized separately but can be utilized simultaneously.

Figure 7 is a schematic diagram of an exemplary vertical die chip-on-board sensor package where an array of I/O pads 702 is arranged on the second face of a vertical sensor circuit component (analogous to section C of Figure 3 ~~Figure 3 (C)~~), in this exemplary case orthogonal to the sensitive direction of the vertical sensor circuit component.

Please amend the abstract to the specification at page 32, line 1 to line 5 to read as follows:

Methods and apparatus for vertical die chip-on-board sensor packages ~~are provided. Such vertical die chip-on-board sensor packages~~ can comprise a vertical sensor circuit component comprising a first face, a second face, a bottom edge, a top edge, two side edges, input/output (I/O) pads and at least one sensitive direction wherein the I/O pads are arranged near the bottom edge.

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